REMARKS

Claims 1-6 have been rejected on grounds on anticipation. In view of the amendments above and the remarks below, Applicant requests reconsideration and allowance.

There are three separate anticipation rejections, which will be addressed together.

Claims 1-4 have been rejected under 35 U.S.C. §102(b) as anticipated by Itoh '530 and by Emori '017. Claims 1-6 have been rejected as anticipated by Noble '083. The above amendments respond to and overcome the rejections.

By the foregoing amendment, claims 1 and 4 are modified and claims 2 and 3 are canceled. In the amendment to claim 1, Applicant has made clear that the invention relates to a memory cell having a FET that operates as a gain element, the FET having a first terminal connected to the storage element, a second terminal connected to the second data line and a third terminal selectively connected to one of a first power supply and a second power supply. The FET preferably is symmetrical as to the second and third terminals, allowing them to be interchanged. No reference discloses these connections or that specific FET structure.

New claim 8 also specifies that the FET is symmetrical as to the second and third terminals, allowing them to be interchanged. That is, as related in claims 1 and 7-9, and shown in Fig. 6, the drain and source of the gain transistor preferably are interchangeable. Nothing of the sort is shown in the references.

The architectures specified in claims 1 and 5 coupled with the FET structures of claims 7 and 9 lead to the ability to use an array of the memory cells as per claim 6 and to perform pivot operations and bit interleaving, using minimum real estate and complexity. None of the references discloses such an apparatus (e.g., the gain FET having interchangeable source and drain) or its use to enable the method of claim 6.

New claims 11 – 13 are identical to respective claims 1 and 7-8 except that the open term "comprising" of claim 1 has been changed to a substantially closed term "consisting essentially of" in claim 11.

With respect to claim 6, reconsideration is requested. The Examiner has rejected the claim as anticipated by Noble and has made a statement that the first select signal line and the second select signal line of Noble are orthogonally disposed. Whether that statement is true or not is irrelevant; the statement does not address or meet the limitations of claim 6. Claim 6 calls for a method of addressing an array of memory cells wherein there are two steps or acts: (1)

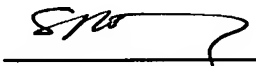
writing groups of bits linearly arrayed with respect to each other; and (2) reading groups of bits linearly arrayed with respect to each other and orthogonally disposed to the groups of bits written. It is not seen that such method is taught in Noble and the Examiner has not shown where it is taught. Accordingly, the rejection lacks *prima facie* support and should be withdrawn. Applicant should not have to guess how the Examiner reads the claims against the reference; it should be stated where the Examiner finds the recited acts in the reference. (Therefore, should the rejection be maintained, the next Office Action should be a non-final action explaining the rejection.)

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,



Steven J. Henry
Reg. No. 27,900
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
(617) 646-8000

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